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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,396	06/23/2003	David S. Edrich	NWISP048	1694

22434 7590 02/23/2006

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EXAMINER

EHNE, CHARLES

ART UNIT	PAPER NUMBER
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2113

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/602,396	Applicant(s) EDRICH, DAVID S.	
	Examiner Charles Ehne	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-33 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10, 12-16, 18, 20-33 is/are rejected.
- 7) ☒ Claim(s) 11, 17 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,2,6-10,12,13,15,18,20,23,24,27-30 and 33 are rejected under 35 U.S.C. 102(b) as being anticipated by Murthi (5,673,388).

As to claim 1, Murthi discloses a input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors (Abstract, lines 4-7 & column 5, lines 6-7).

As to claim 2, Murthi discloses a BIOS of claim 1 wherein one of the plurality of processors comprises a boot strap processor, the computer program instructions being operable to cause the boot strap processor to assign each of the different portions of the system memory to one of the selected processors (column 7, lines 44-49).

As to claim 6, Murthi discloses a BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to instruct the selected processors to begin testing of the system memory (column 7, lines 54-57).

As to claim 7, Murthi discloses a BIOS of claim 6 wherein the computer program instructions are operable to cause each of the selected processors to initialize and validate its assigned portion of the system memory (column 7, lines 54-67).

As to claim 8, Murthi discloses a BIOS of claim 7 wherein the computer program instructions are operable to cause each of the selected processors to report memory testing progress to the boot strap processor (column 8, lines 5-7).

As to claim 9, Murthi discloses a BIOS of claim 8 wherein the computer program instructions are operable to cause each of the selected processors to report the memory testing progress by writing to a field in shared memory associated with the boot strap processor (column 7, lines 35-38).

As to claim 10, Murthi discloses a BIOS of claim 8 wherein the computer program instructions are operable to cause each of the selected processors to update the memory testing progress periodically (column 6, lines 6-12).

As to claim 12, Murthi discloses the BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to monitor progress in testing of the system memory by the selected processors (column 8, lines 16-19).

As to claim 13, Murthi discloses the BIOS of claim 12 wherein the computer program instructions are operable to cause the boot strap processor to periodically update status information corresponding to the progress (column 6, lines 6-12).

As to claim 15, Murthi discloses the BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to generate

memory testing results upon completion of the testing of the system memory by the selected processors (column 6, lines 13-17).

As to claim 18, Murthi discloses the BIOS of claim 2 wherein the computer program instructions are operable to cause the boot strap processor to allocate separate stack memory in a shared memory for each of the selected processors (column 7, lines 57-67).

As to claim 20, Murthi discloses the BIOS of claim 2 wherein the computer program instructions are operable to associate a lock prefix with instructions targeting a shared memory associated with the boot strap processor thereby ensuring that two of the processors do not access the shared memory at the same time (column 3, lines 10-20).

As to claim 23, Murthi discloses the BIOS of claim 1 wherein the computer system comprises a bus for interconnecting the plurality of processors and the system memory, the computer program instructions being operable to facilitate testing of the memory via the bus (Figure 1, column 3, lines 1-3).

As to claim 24, Murthi discloses a computer system comprising a plurality of processors, a system memory, and a basic input/output system (BIOS) embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors (Abstract, lines 4-7 & column 5, lines 6-7).

As to claim 27, Murthi discloses the computer system of claim 24 further comprising a bus for interconnecting the plurality of processors and the system memory (Figure 1, column 3, lines 1-3).

As to claim 28, Murthi discloses a basic input/output system (BIOS) for use in a computer system having a plurality of processors, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous operation of selected ones of the plurality of processors (column 3, lines 27-35 & column 5, lines 6-7).

As to claim 29, Murthi discloses a BIOS of claim 28 wherein the computer system also comprises system memory, the computer program instructions being operable to facilitate substantially simultaneous testing of different portions of the system memory by the selected processors (column 3, lines 27-35).

As to claim 30, Murthi discloses a computer system comprising a plurality of processors and a basic input/output system (BIOS) embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous operation of selected ones of the plurality of processors (column 3, lines 27-35 & column 5, lines 6-7).

As to claim 33, Murthi discloses a computer system of claim 30 further comprising a bus for interconnecting the plurality of processors (Figure 1, column 3, lines 1-3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthi taken in view of Brock (6,421,775).

As to claim 3, Murthi discloses a input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors (Abstract, lines 4-7 & column 5, lines 6-7). Murthi fails to disclose the bios wherein the plurality of processors that are configured in a plurality of processor clusters, each of the clusters corresponding to at least one of the different portions of the system memory.

Brock discloses a data processing system that includes a plurality of processing nodes, that each contains at least one processor (column 2, lines 30-33). The nodes are further connected to a shared memory (column 2, lines 35-41). Brock does disclose the bios wherein the plurality of processors that are configured in a plurality of processor clusters, each of the clusters corresponding to at least one of the different portions of the system memory (column 2, lines 30-33 & column 7, lines 34-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement the plurality of processor clusters and each of the clusters corresponding to at least one of the different portions of the system memory with Murthi's memory testing system. A person of ordinary skill in the art would have been motivated to make the modification because Murthi states there is a need for a faster way to initialize a multiple processor computer system (Murthi: column 2, lines 11-12) and Brock provides a system that addresses the limitations of an SMP computer system (Brock: column 1, lines 43-57).

As to claim 4, Murthi discloses the BIOS of claim 3 wherein each of the processors in each of the clusters has one of the different portions of the system memory associated therewith, the computer program instructions being operable to cause the boot strap processor to assign each of the different portions of the system memory to its associated processor (Figure 3, column 7, lines 44-49).

As to claim 5, Murthi discloses the BIOS of claim 3 wherein the computer program instructions are operable to cause the boot strap processor to assign only one

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of the processors in each cluster to the corresponding portion of the system memory (column 3, lines 49-52).

Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murthi taken in view of Cox (5,357,621).

As to claim 16, Murthi discloses a input/output system (BIOS) wherein the computer program instructions are operable to cause the boot strap processor to generate memory testing results upon completion of the testing of the system memory by the selected processors (column 6, lines 13-17). Murthi fails to disclose wherein the computer program instructions are operable to cause the boot strap processor to disable any memory modules corresponding to corrupted memory ranges indicated in the memory testing results.

Cox discloses a memory system including the capability to disable and bypass bad memory modules (Abstract, lines 12-15). Schelling discloses disabling any memory modules corresponding to corrupted memory ranges indicated in the memory testing results (column 3, lines 23-27).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement disabling any memory modules corresponding to corrupted memory ranges indicated in the memory testing results with Murthi's memory testing system. A person of ordinary skill in the art would have been motivated to make the modification because the system allows removing or disabling the corrupt memory modules without leaving usable memory unallocated (Cox: column 3, lines 38-40).

Claims 21,22,25 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthi taken in view of Dove (5,938,765).

As to claim 21, Murthi discloses a input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors (Abstract, lines 4-7 & column 5, lines 6-7). Murthi fails to disclose wherein the computer system comprises a plurality of point-to-point links interconnecting the plurality of processors.

Dove discloses an apparatus for initializing a shared memory, multi-node multiprocessor computer (Abstract, lines 1-2). Dove does disclose wherein the computer system comprises a plurality of point-to-point links interconnecting the plurality of processors (column 4, lines 21-25). It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to the point-to-point links with Murthi's memory testing system. A person of ordinary skill in the art would have been motivated to make the modification because the links offer low latency and are scalable to allow for the addition of more nodes (Dove: column 4, lines 21-25).

As to claim 22, Dove discloses the BIOS of claim 21 wherein the plurality of processors are configured in a plurality of clusters, and the point-to-point links comprise intra-cluster point-to-point links interconnecting the processors within each cluster and inter-cluster point-to-point links interconnecting the clusters (column 4, lines 21-25).

As to claim 25 and 31, Murthi discloses a input/output system (BIOS) for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of different portions of the system memory by selected ones of the plurality of processors (Abstract, lines 4-7 & column 5, lines 6-7). Murthi fails to disclose wherein the computer system comprises a plurality of point-to-point links interconnecting the plurality of processors.

Dove discloses an apparatus for initializing a shared memory, multi-node multiprocessor computer (Abstract, lines 1-2). Dove does disclose wherein the computer system comprises a plurality of point-to-point links interconnecting the plurality of processors (column 4, lines 21-25). It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to the point-to-point links with Murthi's memory testing system. A person of ordinary skill in the art would have been motivated to make the modification because the links offer low latency and are scalable to allow for the addition of more nodes (Dove: column 4, lines 21-25).

Claims 26 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murthi and Dove as applied to claims 24 and 31 above, and further in view of Brock.

As to claims 26 and 32, Murthi and Dove disclose a an input/output system for use in a computer system having a plurality of processors and a system memory, the BIOS being embodied in a computer readable medium as computer program instructions which are operable to facilitate substantially simultaneous testing of

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different portions of the system memory by selected ones of the plurality of processors. The system comprises a plurality of point-to-point links interconnecting the plurality of processors (See claim rejections 25 and 31). The combination fails to disclose the system wherein the plurality of processors are configured in a plurality of clusters, and the point-to-point links comprise intra-cluster point-to-point links interconnecting the processors within each cluster and inter-cluster point-to-point links interconnecting the clusters.

Brock discloses a data processing system that includes a plurality of processing nodes, that each contains at least one processor (column 2, lines 30-33). The nodes are further connected to a shared memory (column 2, lines 35-41). Brock also discloses a plurality of processors are configured in a plurality of clusters (column 2, lines 30-33 & column 7, lines 34-45).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to implement the plurality of processor clusters and each of the clusters corresponding to at least one of the different portions of the system memory with the combination of Murthi's and Dove's memory testing systems. A person of ordinary skill in the art would have been motivated to make the modification because Murthi states there is a need for a faster way to initialize a multiple processor computer system (Murthi: column 2, lines 11-12) and Brock provides a system that addresses the limitations of an SMP computer system (Brock: column 1, lines 43-57).

Allowable Subject Matter


Claims 11,17 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles Ehne whose telephone number is (571)-272-2471. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


ROBERT BEAUSOLIEL
SUPERVISOR
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